Application of Artificial Neural Networks with Activation Function in Reconfigurable Environment

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ABSTRACT

Nowadays, the battery powered mobile devices are used all over the world for every usage. Hence it enables the backbone of the current communication technology. The neural networks were competent to solve the complex tasks. Different from the customary method, unambiguous algorithm is not necessary. The Artificial Neural Network (ANN) is to provide an enhanced way for computing mathematical functions. It determines that all the low power methods decrease the leakage power moderately. Artificial neural networks are bio-inspired simulations used generally in the problems clarification with nonlinear performance. Reconfigurable devices (FPGA) are extensively laboring in the application of artificial neural networks. The influence of this effort is in the execution of a Multilayer ANN with neurons, one concealed layer and hyperbolic departure for motivation function. Nonlinear function estimation achieved for system endorsement of artificial neural network. This proposed system creates exploration of certain consequences with several methods to operation of the motivation function in Artificial Neural Networks.

Keywords: *Artificial Neural Networks, Reconfigurable devices, Multilayer ANN, Nonlinear function estimation.*

1. INTRODUCTION

Artificial Neural Networks (ANN) are general between scientists, particularly for provide the growth with similar processing methods, strength in the consequences and wide range of applications in automation, image processing, mechanization and control, among others. It often is used in resolving nonlinear complications and real-time applications, which mathematical model is affluent for hardware application. The use of FPGA to implement in hardware ANN has improved, manly by performance related with a high level of parallelism and elasticity provided by reconfigurable devices. Three features are necessary in the development of ANN in reconfigurable device, data demonstration, type of design and method for nonlinear motivation function (AF). Artificial Neural Networks (ANN) are composed of these artificial neurons, usually inclined in layers and associated so as to form networks. Several complications in the field of pattern appreciation, image processing and medical analytic etc. can be determined by Artificial Neural Network. The physically motivated ANNs are similar and disseminated information processing systems. A principal feature of Artificial Neural Networks is their learning capability. Size and real time considerations show that on-chip learning is necessary for a large range of solicitations. In contrast to software application of the network, hardware implementation affords a high level of parallelism. This permits us to make several calculations simultaneously in order to have a higher handling speed. In calculation, the hardware implementation is extremely convenient since it has least necessities in area and power consumption, and provides unrelated. Currently the growth of intellectual and more natural advanced devices, without need of information for restrictions setting action, is motivating the research groups worldwide. The requirement is to have learning and adaptive ability for such smart devices can be gratified using neural networks hardware and software implementation. Thus this paper goal is to help the scholars to recognize the connections in learning about the artificial neural network.

In the design of CMOS, the causes of power consumption primarily due to dynamic power dissipation and leakage power dissipation. Leakage power consumption is a significant concern in CMOS circuit. The main influence of Power dissipation in CMOS circuit rises with the declination of channel length, threshold voltage and gate oxide thickness. The power dissipation of a reason gate is given by

$$P_{avg\ /gate} = P_{switching} + P_{short\ circuit} + P_{leakage}$$

Where

$P_{switching}$ - power dissipated due to charging and discharging of the circuit capacitances,

$P_{shortcircuit}$ is the power dissipated due to the short circuit between V_{dd} and ground during output transitions and

$P_{leakage}$ is the power dissipated due to leakage current.

2. RELATED WORK

Salem M. Elkhodary et.al (2006) proposed **The Use of Experimental and Artificial Neural Network Technique to Estimate Age against Surface Leakage Current for Non-ceramic Insulators.** This paper introduces an experimental and analytical technique to predict the insulator life time, and presents an experimental measurement of the surface leakage current against time of non-ceramic insulators on naturally aged insulators and artificially contaminated material. The study of the leakage current dependence on the insulators contamination level is also presented in this paper. Different prototype of artificial neural networks-based scheme that can estimate the insulator age under different contagion level at the surface of polymer insulators by employing the experimentally calculated leakage current was constructed in this paper. The proposed prototype is trained for different filler level for different insulator type in the neural network. The proposed technique is considered to be helpful tool in the area of quality control.

A.S. Orgenci et.al (2002) proposed **Fault-tolerant training of neural networks in the presence of MOS transistor mismatches.** In this paper, Analog techniques are desirable for hardware implementation of neural networks due to their numerous advantages such as small size, low power, and high speed. However, these advantages are often offset by the difficulties in the training of analog neural network circuitry. In particular, training of the circuitry by software based on hardware models is impair by statistical differences in the integrated circuit production process, resulting in performance degradation. In this paper, a new paradigm of noise vaccination during training for the reduction of this degradation is presented. The differences at the outputs of analog neural network circuitry are modeled based on the transistor-level mismatches occurring between identically designed transistors. Those differences are used as additive noise during training to increase the fault tolerance of the trained neural network.

Omar Banimelhem et.al (2012) proposed **Neural network based optimization of CMOS transistor sizing for leakage power minimization.** This paper introduces reduction of power dissipation makes an electronic device more efficient and reliable. The require for a device that disperse less power was the inspiration for the development of CMOS technology. A novel technique for optimizing electronic circuits by resizing transistor parameters using single perceptron neural network is future. Simulation results have shown that the neural network based approach used in transistor resizing exhibits better ease, better optimization of compound circuits and less computational requirements. The average improvement of leakage power reduction is about 32% for C17 circuit which was simulated assuming 22 nanometer technologies.

M. Manbachi et.al (2014) proposed **Predictive algorithm for Volt/VAR optimization of distribution networks using Neural Networks**. In this paper, Smart Grid functions such as Advanced Metering

Infrastructure, Pervasive Control and Distribution Management Systems have brought numerous control and optimization opportunities for distribution networks through more accurate and reliable techniques. This paper presents a new predictive approach for Volt/VA Optimization (VVO) of smart distribution systems using Neural Networks (NN) and Genetic Algorithm (GA). The future predictive algorithm is able of predicting the load profile of target nodes a day ahead by employing the historical metrology data of Smart Meters, It can further execute a comprehensive VVO in order to minimize distribution network loss/operating costs and run Conservation Voltage Reduction (CVR) to save more energy.

3. ARTIFICIAL NEURAL NETWORK

Artificial neural networks (ANN) have established extensive distribution in a broad spectrum of classification, observation, suggestion and control applications. Any kind of typical data can be classified by using the hardware implementation. More modern networks are a bit freer flowing in terms of stimulation and inhibition with relations interacting in a much more chaotic and complex fashion. One new approach is using relations which span much further and link processing layers rather than always being localized to adjacent neurons. The ANN was developed in programming language of high-level with the Mat lab (without toolbox). The Mat lab has the function of data preparation and comparison of the results between hardware and software. The designer is helped in the optimal of constituents of low-level with growth in high-level. The application and evaluation of the system was completed in level high and low of perception. The outcomes acquired in hardware by the practical simulation were cracked in high-level to produce the consequent results. The analysis of the results is offered in the practice of errors and area usage. Consequences were acquired for different applications of ANN, particularly in varying the AF.

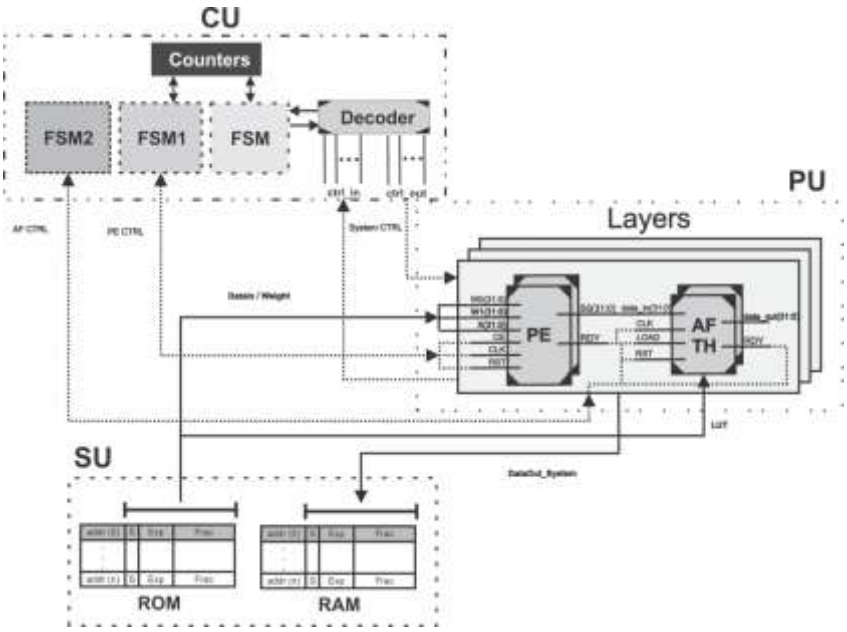

Fig.1. System Architecture of ANN

- **Control Unit**

The ANN course of data is not confessed complications caused by simultaneous execution of processes, e.g., the productivity of one layer cannot be substituted before of be developed by next layer. The CU is in authority by accurate execution of the data flow in the ANN through counters and three state mechanisms. Every state has its output only restructured during the implementation of the state by way of a permit ready signal. The circumstances also consist of a reset signal to avoid the propagation of unwanted values in other times, different of the global signal.

➢ **Storage Unit**

SU contains retentions type surrounded used in the system, but generally select depend on the producer and the family of FPGA. The system hires two different types of BRAM memory, a read only and one for data writing. Both technologies use memory type for single port access data. The ROM type retention is connected to the input data and the activation function. The results are deposited in RAM to permit future transfers on buses. The words in the memory use single precision (32 bits). The output data of the system are stored in file by way of functional simulation for read and compare the results.

➢ **Processing Unit**

Processing Uni**t** comprises the biased sum of the inputs and the masses related with the neuron. FPU based on an IP Core is used to do this processing. PU creates the data calculating in neuron through two main parts AF and PE. The number of constituents in the system is openly linked with the number of inputs to each neuron and number of neurons in a given layer and the amount of layers of ANN.

➢ **Processing Element**

The PE is constrained to a multiplier and an adder in floating point, further than control constituents between the intellection levels. The new inclusion of treating elements depends on the quantity of accesses related with neuron. To have better control of processing component was essential generating a configuration that classifies the enclosure of inputs and outputs in the segments of floating point operations.

➢ **Activation Function**

Nonlinear AF is difficult to be made openly in circuits or low-end application hardware. On the other hand, the benefit in its use is the high accuracy and strength of the network results creating its employ essential for applications that demanding accuracy more sophisticated.

4. RESULTS AND DISCUSSION

The structural design for calculation of the neuron was similar apart from for the AF. Therefore, in all instigated architectures the runtime is the same, since all AF spend two clock cycles. The total runtime in the ANN system is straightly connected to Processing Unit.

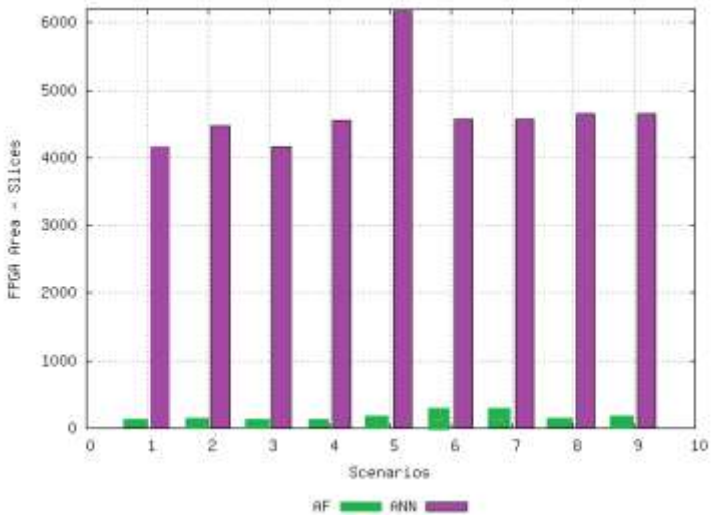

Fig.5. Area Utilization in the Artificial Neural Network system

Fig. 5 concludes the area usage design for the motivation task and system. In the consequences of the scenarios present a relationship in the area usage and precision. But the same setups have had related to the values in the full system, that uses more assets of the FPGA owing to the extent of elements for planning. The mixture effects were accomplished three times at least. Some scenarios used one and four keen memory separately in the system of ANN. There are different quantities of features in the set of data accessible in the LUT, thus the truncation have to be confirmed agreeing with the implementation for an appropriate analysis. Runoff and underflow concessions were omitted in the exploration of the errors, when required. The relationship between the applications on FPGA with the ideal value comprises sufficient validation with low error rate. The implementations results in the system existing a suitable hardware with floating point.

CONCLUSION

The Artificial Neural Network comprises of neurons and hyperbolic angle function in all neurons; all applications into reconfigurable device were sufficient to provide exactness high in the system. The estimates made in the HT role with reasonable results and high data precision, when associated with ultimate result. The high accuracy with low use of reasonable possessions in resembling HT. AF were pleasing contain a slight benefit concerning the usage of combinational circuit and the best adjustment between area and precision. The estimates revealed ability to perform with excellence in implementations of Artificial Neural Network. The model of system on a different platform can be made just with incorporating the components and regarding their definite structures, for take portability and intensifying to the system.

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